Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

(1)-(9) (cancelled)

(10) (currently amended) The microcontroller of claim [1] 18 further comprising a random access memory unit which is communicatively coupled to said micro-control unit.

(11) (original) The microcontroller of claim 10 further comprising a read-only memory unit which is communicatively coupled to said micro-control unit.

(12) (original) The microcontroller of claim 11 wherein said micro-control unit comprises a microprocessor.

(13)-(17) (cancelled)

(18) (original) A single integrated circuit microcontroller having self-erase read protection, comprising:

a flash memory unit containing a read protection flag;

a processing unit;

a plurality of input/output pins;

at least one switching circuit which is adapted to selectively connect and disconnect said plurality of input/output pins to and from said flash memory unit and said processing unit;

a special mode detection circuit which is communicatively coupled to said at least one switching circuit and said plurality of input/output pins, said special mode detection circuit being adapted to detect when a special mode is activated, and to selectively generate a first signal and a second signal when said special mode is activated, wherein said second signal is communicated to said at least one switching circuit, effective to connect said plurality of input/output pins to said flash memory unit only when said special mode is activated; and

a flash memory control circuit which is communicatively coupled to said special mode detection circuit, and which is adapted to receive said first signal, to check said read protection flag upon receipt of said first signal, to erase said flash memory unit and clear said read protection flag if said read protection flag is set and said special mode is activated, and to communicate a third signal to said special mode detection circuit when said read protection flag is cleared and said special mode is activated;

wherein said third signal is effective to cause said special mode detection circuit to generate said second signal only after receipt of said third signal, thereby preventing said plurality of input/output pins from being connected to said flash memory unit unless said special mode is activated and said read protection flag is cleared.

(19) (original) The microcontroller of claim 18 wherein said special mode detection circuit is adapted to detect a special mode by sensing a predetermined sequence of signals on said plurality of input/output pins.

(20)-(26) (cancelled)